



CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies: Process-Aware SRAM Design and Test (Frontiers in Electronic Testing)

Andrei Pavlov, Manoj Sachdev

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The monograph will be dedicated to SRAM (memory) design and test issues in nano-scaled technologies by adapting the cell design and chip design considerations to the growing process variations with associated test issues. Purpose: provide process-aware solutions for SRAM design and test challenges.

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